AEROSPACE REPORT NO.
TOR-2010(8591)-10
REV A

Digital Application-Specific Integrated Circuit and Field-Programmable Gate Array Circuit Development Standard for Space Systems

December 20, 2010

Craig V. Sather, Christine M. Rink, and James M. Dixon
Digital and Integrated Circuit Electronics Department
Electronics Engineering Subdivision

Prepared for:

Space and Missile Systems Center
Air Force Space Command
483 N. Aviation Blvd.
El Segundo, CA 90245-2808

Contract No. FA8802-09-C-0001

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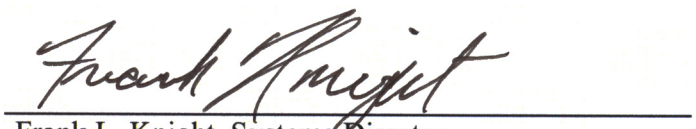

Frank L. Knight, Systems Director
Systems Engineering Directorate
Engineering and Integration Division
Space Systems Group

Foreword

This standard provides requirements for the planning, development, implementation, verification, and maintenance of circuitry applied to digital Application-Specific Integrated Circuits (ASICs) and Field-Programmable Gate Arrays (FPGAs) used in space systems.

Acknowledgements

A group of ASIC/FPGA developers from the aerospace industry were asked to critique the original edition (March 2010) of this standard and each of the respondents provided constructive improvement recommendations to the authors. The changes resulting from our –the author's – review and disposition of those recommendations are incorporated into this second edition of this standard. We are grateful for the "extra mile" of effort each of the reviewers provided and appreciate their individual and collective contributions towards improving this standard and easing its application in our industry.

External contributors to the second edition this standard include:

Ball Aerospace	Mike McDonnell
ITT Geospatial Systems	Daniel J. Bielat; Michael G. Fairchild; Gordon F. Lupien**,** Jr.
Lockheed-Martin Space Systems	Robin Gee
Northrop Grumman Aerospace Systems	
Raytheon Space and Airborne Systems	Noel Ellis

Contents

1. Scope

This standard provides uniform requirements for digital ASIC (Application-Specific Integrated Circuit) and FPGA (Field-Programmable Gate Array) circuit development process activities. These requirements are applicable to the entire life cycle of digital integrated circuit design planning, development, verification, and maintenance.

The technical requirements encompassing the scope of this standard are partitioned into two groups: General requirements and detailed requirements. This standard also includes non-technical requirements, found in Appendix A, that specify fundamental content for technical documents produced in compliance with this standard. The General requirements in this standard, which are contained in section 4, have a scope that covers the fundamental engineering process activities and integral supporting processes and services that apply across the digital ASIC and FPGA circuit design planning development, verification, and maintenance lifecycle. The detailed requirements in this standard, which are contained in section 5, have a scope covering ASIC and FPGA planning, development, verification, technical documents, and maintenance. An overview of the breadth of activities and resulting engineering artifacts covered by the detailed requirements is in Appendix B.

1.1 Application

This standard applies to the planning, development, modification, verification and maintenance of digital circuitry:

a. Intended for use in one or more digital ASIC and/or FPGA;
b. Intended for use in the digital portion of a mixed signal device.

1.1.1 Contract Specific Application

This standard is invoked by citing it in a contract. It applies to each ASIC/FPGA digital circuit design module, and each ASIC and/or FPGA circuit design covered by the contract; and, unless otherwise specified in the contract, this standard applies to the prime contractor and all development team members (e.g., associate contractors, subcontractors).

The acquirer is expected to specify the ASIC/FPGA circuit usage category(s) to which this standard applies (e.g., flight equipment, support equipment, ground equipment). When a usage category is not specified by the contract, this document applies to digital circuitry intended for use in or being used in flight equipment.

1.1.2 Tailoring

This standard can be tailored for each type of ASIC/FPGA circuit to which it is applied. While tailoring is the responsibility of the acquirer, prospective and selected developers may provide suggested tailoring. General tailoring guidance can be found in section 6.4.

1.2 Order of Precedence

In the event of conflict between the requirements of this standard and other applicable standardization documents, the acquirer is responsible for resolving the conflicts.

2. Applicable Documents

2.1 General

The documents listed below are not necessarily all of the documents referenced herein, but are those needed to understand the information provided by this standard.

2.2 Government Documents

2.2.1 Specifications, Standards, and Handbooks

The following specifications, standards, and handbooks form a part of this document to the extent specified herein.

a. none

2.3 Non-Government Publications

The following documents form a part of this document to the extent specified herein.

a. none

3. Definitions

Acquirer: An organization that procures products for itself or another organization.

AFDP: ASIC/FPGA development plan.

AFER: ASIC/FPGA emulation report.

AFSS: ASIC/FPGA system specification.

APIR: ASIC/FPGA system and parent item integration report.

ASIC: Application-Specific Integrated Circuit.

Associate developer: An organization that is neither prime contractor nor subcontractor to the developer, but who has a development role on the same or related system or project.

CDAR: Circuit Design Analysis Report.

CDRL: Contract Data Requirements List. Deliverable data required by a contract that typically has its content specified by a DID.

CRR: Consolidated Requirements Review.

Data item description (DID): The format and content preparation instructions for a data product generated by the specific and discrete task requirement as delineated in the contract.

Developer: An organization responsible for developing one or more ASIC and/or FPGA products covered by the contract.

End item: A deliverable product or a discrete, qualifiable part of a deliverable product (such as an On Board Computer unit, payload data processing unit or a router) that will perform a system mission function.

Product development library: An organized, controlled repository of material used by and produced by the ASIC/FPGA development team members.

FRR: Final Requirements Review.

FPGA: Field-Programmable Gate Array.

IP: Intellectual property.

Parent item: Discrete or aggregate set of equipment that is hierarchically above, directly interfaces with, and whose performance is dependent upon the subject ASIC/FPGA.

PIR: Parent item Integration Report.

Processor firmware: Processor software within a non-reprogrammable or reprogrammable non-volatile hardware device.

Processor software: Processor instructions and/or data used to operate a processor (e.g., micro-processor).

PLD: Programmable logic device. An FPGA is a type of PLD.

QTR: Qualification test report.

Qualification testing: Testing performed to demonstrate to the acquirer that an ASIC/FPGA system, independent ASIC/FPGA, and/or its parent item meets its specified requirement.

Requirement: a) A characteristic that an ASIC/FPGA, ASIC/FPGA system, and/or parent item must possess in order to be acceptable to the acquirer; b) A mandatory statement in a standard or another portion of the contract.

RVTM: Requirements verification and traceability matrix.

SRR: System requirements review.

Software item: An aggregation of software that satisfies an end use function and is designated for purposes of specification, interfacing, qualification testing, configuration management, or other purposes. Software items are selected based on tradeoffs among software function, size, host or target computers, developer, support strategies, plans for reuse, criticality, interface considerations, need to be separately documented and controlled, and other factors. A software item is comprised of one or more software units. A software item is sometimes called a computer software configuration item (CSCI). [Reference: SMC-S-012; *Software Development for Space Systems*].

Type I ASIC/FPGA: A single ASIC or FPGA having a design that does not contain an embedded processor.

Type II ASIC/FPGA: A single ASIC or FPGA having a design that contains an embedded processor; or, two or more ASIC and/or FPGA devices that are developed jointly and intended to directly interface with one another. This type of design configuration and associated complexity is often referred to as a system, a system on a chip, or in the case of multiple devices - a chip set.

4. General Requirements

This section identifies the fundamental engineering process activities and integral supporting processes and services that apply across the digital ASIC and FPGA circuit design planning, development, verification, and maintenance lifecycle.

The developer shall satisfy the following general requirements in implementing the detailed requirements described in Section 5 of this standard.

4.1 Digital ASIC and FPGA Circuit Development Process Activities

The developer shall establish ASIC and FPGA circuit development processes that are appropriate to the item(s) being developed, are systematic and consistent with documented industry best practices, and include process activities and products that will satisfy the contract requirements. If soft products (e.g., source code and documentation) only are being developed to satisfy the contract requirements, then some of the following activities may not be applicable. Otherwise, these activities may overlap, be applied iteratively, or be expanded from the following.

a. General requirements for digital ASIC & FPGA circuit development (Section 4.2)
b. Project planning, preparation and coordination (Section 5.1)
c. Parent item and relevant requirements analysis and flow-down (Section 5.2)
d. ASIC/FPGA requirements and architecture definition (Section 5.3)
e. ASIC/FPGA circuit development and verification (Section 5.4)
    1) Circuit source code development
    2) Early verification of procured IP
    3) Circuit verification source code development
    4) ASIC/FPGA circuit implementation, emulation and analysis
f. Design verification (Section 5.5)
    1) ASIC/FPGA interface circuit analysis
    2) Type II ASIC/FPGA emulation and demonstration
g. End item ASIC/FPGA integration and qualification (Section 5.6)
h. FPGA post-qualification changes and verification (Section 5.7)
i. Peer reviews (Section 5.8)
j. Subcontractor management (Section 5.9)

4.2 General Requirements for Digital ASIC and FPGA Circuit Development

4.2.1 ASIC/FPGA Development Methods

The developer shall use systematic, documented methods for all ASIC/FPGA development activities.

The people implementing these documented methods shall be familiar with the methods, have training or experience applying them, and have access to the relevant documentation.

Any tailoring of the developer's ASIC/FPGA development methods (e.g., command media) applied to the subject project shall:

a. Remain consistent with best practices
b. Be documented
c. Be approved by the developer's responsible project leadership
d. Be communicated to and made available to the engineering team and the acquirer

4.2.2 ASIC/FPGA Development Tools

The developer shall use development tools that have been previously integrated into and demonstrated in a relevant application by developer personnel. In addition, development team members using the tools shall be familiar with the applied development tool suite and have training or experience using them in a relevant application.

4.2.3 Traceability

The developer shall perform, document, and maintain bi-directional traceability between the parent item requirements and each level of hierarchy down to individual ASIC and FPGA requirements.

For each Type I and Type II ASIC/FPGA, derived design requirements stemming from design decisions, and verification cases stemming from verification decisions, shall be traceable to documentation describing those design and verification decisions.

The purpose of establishing and maintaining documented traceability is to trace both upward and downward to ensure that all requirements (explicit and derived) are implemented and verified; and, to ensure that associated design and verification decisions remain identifiable and consistent across the development lifecycle.

4.2.4 Assurance of Critical Requirements

The developer shall define and document their approach to satisfy the following types of critical requirements:

a. Safety: prevention and/or control of circuit erroneous behavior and/or performance characteristics that could lead to one or more human or equipment safety hazards;

b. Security: prevention, mitigation, and/or control of revealing circuit implementation, architecture, behavior and/or performance characteristics that could lead to a violation of one or more explicit or derived security requirements;

c. Privacy: prevention, mitigation, and/or control of revealing of circuit behavior and/or performance characteristics that could lead to a violation of explicit or derived privacy requirements;

d. Other mission-critical requirements (e.g., survivability, reliability) as agreed to by the acquirer and the developer(s).

4.2.5 Documenting Key Decisions

Key Type I and Type II ASIC/FPGA development planning decisions made by the developer regarding device technology selection or the specification, design, implementation, verification, and/or maintenance of ASIC/FPGA circuit design(s) shall be documented and archived in a product development library (Section 5.1.2).

4.2.6 Reusable ASIC/FPGA Circuit Definitions

The developer shall determine if reusable circuit definitions (inclusive of commercially available intellectual property (IP) are available and of sufficient quality and performance characteristics to satisfy or efficiently aid the satisfaction of contract requirements.

All reusable circuit definitions applied to the ASIC/FPGA development and the criteria used to evaluate their acceptability shall be listed (along with any related data rights) in the ASIC/FPGA development plan (Section 5.1.1) and traceable to respective design decision and associated trade study documentation.

Trade studies used to decide between creating a new circuit definition and the use of reusable ASIC/FPGA circuit definitions, as-is or with modifications, shall assess the benefits of their use with respect to, but are not limited to, the following:

a. Security
b. Maturity
c. Suitability for target device technology
d. Documentation sufficiency
e. Functional and performance characteristics of needed capabilities
f. Sufficiency of previous analyses to satisfy current requirements
g. Cost benefits
h. Schedule benefits
i. Risk of retaining unused circuitry
j. Risk of accepting known deficiencies
k. Risk of modifications

4.2.7 ASIC/FPGA Device Resource Utilization

Device resource utilization metrics (e.g., capacity vs. goal vs. estimated/actual usage; area, gates, look-up tables, routing tracks) shall be monitored, managed, and reported to developer and acquirer technical management during technical reviews and management reviews.

4.2.8 Critical Enterprise Support

The developer shall implement enterprise support services critical to ensuring that development processes are followed, that development products are controlled, and that contractual requirements are satisfied by the developer and any associated developers or subcontractors.

These support services shall include but are not limited to:

a. Project management
b. Configuration management
c. Quality assurance
d. Subcontract management

4.2.9 Integral Processes

4.2.9.1 Risk Management

The developer shall rigorously apply risk management throughout the ASIC/FPGA circuit design development, verification and maintenance lifecycle. Risk management includes the identification, analysis, and prioritization of technical performance, cost, and schedule risks; additionally, it includes the creation and implementation of plans to eliminate or control those risks.

All ASIC/FPGA device, circuit, and development process related technical performance, cost and schedule risks shall be documented and included in technical reviews and management reviews.

4.2.9.2 Corrective Action System

The developer shall implement a corrective action system for handling each problem detected regarding the ASIC/FPGA development process or process execution and each problem regarding ASIC/FPGA requirements, circuit design or related documentation that are under configuration control.

Corrective actions shall be evaluated to determine whether problems have been resolved, adverse trends have been reversed, and changes have been correctly implemented without inducing additional problems.

4.2.9.3 Management and Acquirer Oversight

The developer shall plan and take part in ASIC/FPGA related technical and management reviews.

a. Technical reviews shall be attended by persons with technical knowledge of the parent item and the ASIC/FPGA device and circuit being reviewed.

b. Technical reviews shall be conducted to ensure ongoing communication and foster the exchange of technical information between acquirer and developer technical personnel regarding problems and risks, development metrics, resolving development environment and design and verification issues.

c. Management reviews shall be attended by persons with authority to make cost and schedule decisions and shall include:
    1) Informing management about project status, directions being taken and technical agreements reached
    2) Resolving issues that could not be resolved during technical reviews
    3) Identifying and resolving management-level issues and risks
    4) Obtaining commitments and acquirer approvals needed for timely accomplishment of the project

4.2.10 Access for Acquirer Review

The developer shall provide the acquirer and its authorized representative(s) access to developer and subcontractor facilities, including the ASIC/FPGA engineering and verification environments, for review of ASIC/FPGA circuit development activities and documentation.

5. Detailed Requirements

5.1 Project Planning, Preparation and Coordination

The developer shall perform project planning, preparation and coordination in accordance with the following requirements.

5.1.1 ASIC/FPGA Development Planning

When developing one or more Type I ASIC/FPGA or Type II ASIC/FPGA circuit designs, the developer shall develop and document plans for conducting their respective development activities. The planning shall be consistent with the contract requirements and include but not be limited to the activities identified within this standard.

The purpose of the ASIC/FPGA development planning is to communicate the documented ASIC/FPGA development, acquisition, analysis, integration, verification, qualification, and maintenance approach to the development team, critical enterprise support, and the acquirer.

5.1.1.1 ASIC/FPGA Development Plan

The ASIC/FPGA development planning shall result in a comprehensive development approach described in an ASIC/FPGA Development Plan (AFDP).

Augmented by the AFDP non-technical content required by Appendix A, the AFDP shall include and describe the following:

a. The scope of the development effort

b. The quantity of Type I and Type II ASIC/FPGAs intended to be developed and maintained, each correlated to: a description of its intended application; a description of the device, its technology, and manufacturers name; and the name of the entity responsible for performing for the circuit development

c. The ASIC/FPGA development processes that will be applied, including any tailoring to developer's documented development process (e.g., command media)

d. How the general requirements of this document will be applied to the development, test and maintenance of the ASIC/FPGAs

e. How documents (e.g., trade studies, design decisions, specifications, source code, test) will encompass the documentation requirements of this standard and how they will be controlled and archived

f. The development schedule

g. A comprehensive list of formal and informal reviews correlated to their entrance and exit criteria

h. A comprehensive list of deliverable documentation (draft, preliminary and final versions) correlated to their estimated completion dates

i. A description of the development environment and tool suites that will be used

j. Any special modeling planned

k. Any special testing planned (e.g., radiation, demonstration, certification)

l. The technical performance metrics to be applied, monitored, and reported

The original AFDP and each revision shall be archived in the product development library (Section 5.1.2).

Following acquirer concurrence (approval if required by contract) of the AFDP, the developer shall conduct the relevant activities in accordance with the plan. Updates to the plan shall be subject to acquirer concurrence, unless otherwise specified by the contract.

Section 6.3 contains information regarding the AFDP DID.

5.1.2 Product Development Library

The developer shall establish, control and maintain a product development library that includes all documentation related to and produced during the course of the development of each ASIC and/or FPGA. This documentation shall include but is not limited to applicable specifications, standards, plans, process descriptions, program directives, design decisions, development tool support information, coding guidelines, peer review guidelines, design artifacts, analyses, and reports.

The information in the product development library shall be available to development team members, including the acquirer and their technical representatives. The information in the library shall be maintained for the duration of the contract, unless otherwise specified by the contract.

5.1.3 Design and Development Environment

The developer shall prepare for and ensure that adequate resources (e.g., personnel, workstations, development tools, laboratory tools, and licenses) are provided for the development team to complete their work in time frames consistent with the development plan and contractual requirements.

5.1.4 Associate Developer Coordination

The developer shall coordinate with associate developers, working groups, and interface groups as required to satisfy the contract.

5.2 Parent Item and Relevant Requirements Analysis and Flow-down

The developer shall analyze the parent item requirements and constraints in conjunction with all relevant additional requirements and constraints. These combined requirements and constraints include but are not limited to the following:

a. Parent item requirements
b. Applicable standards and specifications

c. Applicable compliance regulations and policies
d. Derived requirements
e. Safety, hazard, privacy, maintenance, test, and disposal considerations
f. Enterprise and design constraints
g. Acquirer, user and developer feedback and lessons learned from models, prototypes, and/or previous system development and operational activities

The primary purpose of analyzing the parent item and relevant requirements is to ensure that all applicable explicit requirements and constraints are identified, to gain a comprehensive understanding of them, and to flow-down and document a consolidated set of the applicable explicit requirements in advance of elaborating and establishing the Type I or Type II ASIC/FPGA design and verification requirements. Consequently, a result of the parent item and relevant requirements analysis and flow-down activity is to document a draft version of a Requirements Verification and Traceability Matrix (RVTM) for each Type I and Type II ASIC/FPGA and a preliminary version of an ASIC/FPGA System Specification (AFSS) for each Type II ASIC/FPGA. In addition, a result of the parent item and relevant requirements analysis and flow-down activity is to perform a consolidated requirements review (Section 5.2.3) in advance of developing and finalizing the detailed specification for each Type I and Type II ASIC/FPGA (Section 5.3).

5.2.1 ASIC/FPGA System Specification, Preliminary

For each Type II ASIC/FPGA, the parent item and relevant requirements analysis and flow-down activity shall result in defining and documenting a preliminary version of an AFSS. Augmented by AFSS non-technical content required by Appendix A, a preliminary version of an AFSS shall include the following Type II ASIC/FPGA requirements (performance and verification):

a. All flowed-down explicit requirements

b. All non-functional requirements

c. A preliminary set of the interface (i.e., hardware and any applicable software and/or firmware) requirements

d. A preliminary set of derived functional requirements

Each AFSS requirement shall be assigned a unique identifier.

The completed preliminary AFSS shall be archived in the product development library.

Section 6.3 contains information regarding the AFSS DID.

5.2.2 Requirement Verification and Traceability Matrix, Draft

For each Type I and Type II ASIC/FPGA, the parent item and relevant requirements analysis and flow-down activity shall result in defining and documenting a draft version of a Requirement Verification and Traceability Matrix (RVTM).

NOTE: The RVTM is specified herein to mature incrementally via three progressively cumulative versions: Draft (5.2.2), then Preliminary (5.3.5), then Final (5.4.6). The Draft RVTM should be structured to eventually accommodate the collective content requirements of successive versions.

5.2.2.1 Unique Type I and Type II RVTM Requirements

A draft RVTM shall include the following Type I or Type II requirements (performance and verification):

a. For a Type II ASIC/FPGA draft RVTM: all of the requirements documented in the preliminary AFSS

b. For a Type I ASIC/FPGA draft RVTM: all flowed-down explicit requirements applicable to the Type I ASIC/FPGA; all non-functional requirements applicable to the Type I ASIC/FPGA; a draft set of the interface requirements applicable to the Type I ASIC/FPGA; and a draft set of any derived functional requirements applicable to the Type I ASIC/FPGA.

5.2.2.2 Common Type I and Type II RVTM Requirements

Each requirement (performance and verification) contained in the RVTM shall be assigned a unique identifier. Requirements common to an AFSS and RVTM shall use the same unique identifier.

A draft RVTM shall include bi-directional traceability between the requirements it contains and the following:

a. Parent item requirements
b. Any other relevant requirements
c. Applicable design decisions documented to date

RVTM non-technical content and format requirements are in Appendix A.

The completed draft RVTM shall be archived in the product development library.

Section 6.3 contains information regarding the RVTM DID.

5.2.3 Consolidated Requirements Review (CRR)

The parent item and relevant requirements analysis and flow-down activity shall result in a review of the requirements and associated design decisions and verification methods in the RTVM. A CRR for a Type II ASIC/FPGA shall also ensure that the AFSS requirements are contained within the RVTM. This review is considered a consolidated requirements review (CRR).

The CRR shall be attended by relevant requirement stake holders and development personnel (e.g., project leadership, design and verification engineers). The acquirer shall be invited to attend the CRR.

The developer shall obtain CRR sign-off from each RVTM (and, AFSS) requirement domain stakeholder confirming their satisfaction with the CRR content relevant to the domain for which they are responsible. In addition, the final CRR package, including its approval signatures and any action item results, shall be archived in the product development library.

5.2.3.1 CRR Content and Purpose

The CRR shall be conducted to ensure that all of the draft RVTM (and applicable AFSS) functional, performance, verification, and qualitative requirements are consistent with the contract; complete; understood; and bi-directionally traceable between the RVTM/AFSS requirements and the higher level requirements and associated design decisions. The CRR content shall encompass all of the applicable Type I and Type II ASIC/FPGA circuit and any embedded firmware or software lifecycle (i.e., development; verification, including any certification; maintenance, including design changes and verification leading to on-orbit reprogramming); and pre-deorbit/disposal) requirements. Also, the CRR shall include a summary of results, plans and expectations of the development, verification, and qualification activities that were and will be performed, i.e., requirements analysis, trade studies, development process selection, risk assessments, demonstrations, worst case analyses, tests.

CRR non-technical content and format requirements are in Appendix A.

The original CRR presentation material and any revisions, CRR action items, and CRR action item responses shall be archived in the product development library.

Section 6.3 contains information regarding the CRR DID.

The CRR is conducted as the final review of the consolidated requirements prior to committing significant resources to the detailed development (including verification) of the Type I and/or Type II ASIC/FPGA requirements, circuitry, and any associated software/firmware. The CRR is intended to serve as the forum to confirm that all of the explicit and derived ASIC/FPGA requirements are complete, understood, are flowed down to the correct documentation, and that the requirements can be implemented within a risk range consistent with program objectives and contractual requirements. The CRR is also intended to ensure that the development team understands the context of the ASIC/FPGA development, the development plan activities and time frames within which they are to be completed, any re-programming objectives, and any planned risk and opportunity on-ramps and off-ramps.

5.3 ASIC/FPGA Requirements and Architecture Definition

The requirements documented in the applicable AFSS and RVTM shall be among the primary technical inputs to the ASIC/FPGA requirements and architecture definition activity. Those inputs shall be accompanied with information describing pertinent technologies (e.g., feature size, materials, and processes) that are mature enough to satisfy the requirements and serve as part of the design solution. Consequently, the primary inputs to the design requirements and architecture definition activity include but are not limited to the RVTM, applicable AFSS, and descriptions of ASIC/FPGA solution enabling technologies.

The purpose of the ASIC/FPGA requirements and architecture definition activity is to develop the architectural design and define the design requirements needed to support that architecture. The result of the design requirements and architecture definition activity is to include the following:

a. For Type I and Type II ASIC/FPGA circuit design
    1) Architecture of each ASIC/FPGA

2) Trade studies and design decisions identifying requirements that are to be satisfied by reused designs (including procured designs: aka intellectual property or I.P.)
3) Allocation of requirements to one or more device
4) Preliminary RVTM
5) ASIC/FPGA circuit design specification(s)

b. Additionally for each Type II ASIC/FPGA
1) ASIC/FPGA interface architecture and internal circuit architecture
2) Allocation of requirements to any Type II ASIC/FPGA embedded processor firmware items and/or software items
3) Final AFSS

5.3.1 ASIC/FPGA Device Selection

The developer shall select and use ASIC/FPGA device(s) and technologies that can accommodate the circuitry and satisfy the contract requirements.

Trade studies used for device selection shall include, but are not limited to the following:

a. Technology readiness level
b. Extent of compliance to contractual parts and materials requirements
c. Extent of compliance to environmental requirements
d. Extent of compliance to security requirements (e.g., anti-tamper, trust)
e. Electrical power, grounding, and signaling characteristics
f. Temporal performance characteristics
g. Characteristics regarding logic gate and/or specialized macro-cell functions
h. Packaging characteristics

The design decision capturing the results of the ASIC/FPGA device selection activity shall be documented and archived in the product development library.

5.3.2 ASIC/FPGA Architecture

When developing a Type I or Type II ASIC/FPGA, the ASIC/FPGA requirements and architecture definition activity shall result in a design decision describing and documenting the ASIC/FPGA interface and circuit architecture.

The design decision capturing the results of the ASIC/FPGA architecture activity shall be documented and archived in the product development library.

5.3.3 ASIC/FPGA Circuit Design Specification

The ASIC/FPGA requirements and architecture definition activity shall result in describing, documenting, and archiving in the product development library a circuit design specification for each ASIC and FPGA.

Augmented by its non-technical content required by Appendix A, the ASIC/FPGA circuit design specification shall include:

a. Device Overview
b. Functional Description

c. Performance requirements
d. Physical Characteristics
e. Electrical Information
f. Traceability table, which links the requirements in the circuit specification with the requirements they satisfy in the RVTM

The original ASIC/FPGA circuit design specification and each revision shall be archived in the product development library.

Section 6.3 contains information regarding the ASIC/FPGA circuit design specification DID.

5.3.4 AFSS, Final

When developing a Type II ASIC/FPGA, the ASIC/FPGA requirements and architecture definition activity shall result in a final AFSS that satisfies all of the preliminary AFSS content requirements and also includes all explicit requirements and any elaborated, refined and/or derived Type II ASIC/FPGA capabilities and requirements. All requirements included in the AFSS shall have a unique identifier.

AFSS non-technical content and format requirements are in Appendix A.

The completed preliminary AFSS shall be archived in the product development library.

Section 6.3 contains information regarding the AFSS DID.

5.3.5 RVTM, Preliminary

When developing a Type II ASIC/FPGA, the ASIC/FPGA requirements and architecture definition activity shall result in a preliminary RVTM that satisfies the draft RVTM requirements and includes all of the requirements in the final AFSS. When developing a Type I ASIC/FPGA, the ASIC/FPGA requirements and architecture definition activity shall result in a preliminary RVTM that satisfies the draft RVTM requirements (see 5.2.2) and includes any elaborated, refined or derived ASIC/FPGA architectural level and interface requirements. All requirements in the RVTM shall have a unique identifier.

A preliminary RVTM shall include bi-directional traceability between the requirements it contains and the following:

a. Parent item requirements
b. Applicable design decisions documented to date
c. Architectural components (e.g., devices, SW/firmware)
d. Verification method(s) (e.g., Inspection, analysis, demonstration, test)
e. Verification event (e.g., worst case analysis, qualification)

RVTM non-technical content and format requirements are in Appendix A.

The completed preliminary RVTM shall be archived in the product development library.

Section 6.3 contains information regarding the RVTM DID.

NOTE: A final RVTM (Section 5.4.6) will include contents of the preliminary version and traceability from each requirement to its verification test case(s).

5.3.6 Type II ASIC/FPGA Embedded Processor Software/Firmware Items

When developing a Type II ASIC/FPGA, AFSS requirements traceable to embedded processor software and/or firmware items shall be applied as a set of explicit requirements to their respective software/firmware item requirement documents.

5.3.7 ASIC/FPGA Final Requirements Review

The ASIC/FPGA requirements and architecture definition activity shall result in the conduct of an ASIC/FPGA Final Requirements Review (FRR).

The FRR shall include:

a. Results of the requirements analysis and flow-down
b. Results of architectural design
c. Results of any architectural modeling and analyses
d. Results of applicable trade studies and specialty discipline studies (e.g., ASIC vs. FPGA, on-orbit maintainability and re-programmability assessment, ASIC/FPGA technology readiness assessment, radiation tolerance assessment, resource utilization estimates)
e. A list of ASIC/FPGA development risks and opportunities
f. Overview of development plan progress and plan forward

FRR non-technical content and format requirements are in Appendix A.

The FRR shall be attended by relevant requirement stake holders and development personnel (e.g., project leadership, design and verification engineers). The acquirer shall be invited to attend the FRR.

The original FRR presentation material and any revisions, FRR action items, and FRR action item responses shall be archived in the product development library.

Section 6.3 contains information regarding the FRR DID.

The primary objectives of the FRR are to 1) provide a forum in which to formally review and disposition the sufficiency of the detailed ASIC/FPGA (circuit and device; design and verification) requirements to satisfy the ASIC/FPGA requirements in the RVTM, and 2) gain consensus between project leadership, parent item stakeholders and ASIC/FPGA design and verification implementation engineering personnel that the ASIC/FPGA requirements are correct, complete, understood, capable of being implemented, verifiable, and sufficient to release for development use and configuration control.

5.4 ASIC/FPGA Circuit Development and Verification

5.4.1 Circuit Source Code Development

The circuit-design code development activities shall result in source code that satisfies its circuit design specification requirements and relevant contractual requirements.

5.4.2 ASIC/FPGA Verification Metrics

Verification metrics shall be developed and reported to quantitatively show the extent that circuits have been simulated and/or tested and requirements have been verified.

5.4.3 Early Verification of Procured Complex IP

In advance of integrating vendor provided complex IP with other complex circuit modules, or with final (top level) device integration, the developer shall subject the IP to a comprehensive suite of design verification tests. Findings shall be compared to IP specifications and operational needs; and then, individually dispositioned and documented as acceptable or not.

Any actions taken to reconcile IP features dispositioned as unacceptable shall be documented and reported to technical management.

The results of the early verification of procured complex IP activity shall be documented and archived in the product development library.

5.4.4 ASIC/FPGA Circuit-Verification Source Code Development

The ASIC/FPGA circuit-verification code development activity shall define and develop a suite of tests that verify all of the ASIC/FPGA functional design requirements intended to be satisfied by test and or demonstration.

Circuit model verification tests shall be applied to the originating source code, RTL and gate levels of modeling.

5.4.5 ASIC/FPGA Preliminary Design Review

Preliminary ASIC/FPGA circuit-design shall culminate in a Preliminary Design Review (PDR).

Each ASIC and FPGA PDR shall include:

a. Overview of architecture and circuit module partitioning
b. Device floor plan
c. Device packaging and I/O characteristics (e.g., pin count, signal type, loading, initial timing) versus need
d. Device power consumption versus power requirement and allocation constraint
e. Clocking and reset architecture
f. Resource utilization estimates compared to device utilization capacities, manufacturer's recommended maximum use, and developer's risk threshold metrics (e.g., 80% of manufacturer's recommended maximum)

ASIC/FPGA PDR non-technical content and format requirements are in Appendix A.

The original ASIC/FPGA PDR presentation material and any revisions, PDR action items, and PDR action item responses shall be archived in the product development library.

Section 6.3 contains information regarding the ASIC/FPGA PDR DID.

5.4.6 RVTM, Final

The final RVTM shall satisfy the preliminary RVTM content requirements (see 5.3.5) and be matured to also include:

a. A list containing each requirements to be satisfied by test or demonstration correlated with their respective verification test case(s)

b. A list containing each verification test case correlated to the source code that satisfies the test case.

RVTM non-technical content and format requirements are in Appendix A.

The completed final RVTM shall be archived in the product development library.

Section 6.3 contains information regarding the RVTM DID.

5.4.7 ASIC/FPGA Emulation

In advance of committing to an ASIC or FPGA final circuit design, the developer shall implement the ASIC or FPGA circuit design using one or more FPGA(s) and subject it to a comprehensive suite of design verification tests. The FPGA(s) used shall have performance characteristics that, as closely as possible, are equivalent to the end item ASIC or FPGA. The design verification test configuration shall include item under test interfaces having functional and temporal, including asynchronous, behavior representative of its intended use. Additionally, the ASIC or FPGA circuit definitions used to demonstrate design verification satisfaction shall be the final version of those definitions.

The purpose of the ASIC/FPGA emulation activity is to minimize circuit design risk by ensuring that the ASIC/FPGA performs in satisfaction of its requirements before approving the release of the final design.

5.4.8 FPGA Circuit Implementation

The FPGA circuit implementation activities shall result in design requirement- and contractual requirement-compliant:

a. FPGA circuit analyses
b. FPGA configuration file
c. FPGA Critical Design Review (CDR)

5.4.8.1 FPGA Circuit Analysis

The purpose of the FPGA circuitry analysis activity is to analyze the circuit design implemented in the FPGA internal circuitry to ensure that it meets all FPGA circuit resource constraints, power, timing, and signaling criteria.

The FPGA circuit implementation and circuit analysis activity shall analyze the circuit design and result in:

a. Logic simulations of the design's final configuration

b. Static timing analysis of the final design configuration
c. Reset, clock and clock domain crossing analysis
d. Device packaging and I/O characteristics (e.g., pin count, loading, timing, signaling type, simultaneous switching) versus need
e. Power estimation of the final design configuration

5.4.8.2 FPGA Configuration File

The final FPGA circuit design shall include a documented, released, and configuration management controlled configuration (e.g., bit map) file that has been fully verified to satisfy its requirements.

5.4.8.3 FPGA CDR

The FPGA circuit implementation activity shall conclude with the completion of an FPGA Critical Design Review (CDR).

Each FPGA CDR shall include:

a. Review of final architecture
b. Review of packaging and I/O requirements
c. Review of final power consumption
d. Review of device resource utilization metrics
e. Review of extent that the design will satisfy functional and performance requirements
f. Review of design margins
g. Review of final design for test
h. Review of test metrics
i. Final version description

FPGA CDR non-technical content and format requirements are in Appendix A.

The original FPGA CDR presentation material and any revisions, FPGA CDR action items, and FPGA PDR action item responses shall be archived in the product development library.

Section 6.3 contains information regarding the FPGA CDR DID.

5.4.9 ASIC Physical Design

The ASIC physical design development activities shall result in:

a. ASIC circuit analyses
b. Final artwork description (e.g., GDSII)
c. A formal Critical Design Review (CDR)
d. A verified physical design Release to Manufacturing (RTM)
e. Photolithographic mask generation

5.4.9.1 ASIC Floor Planning

The purpose of ASIC floor planning is to lay the foundation for the ASICs internal architecture, including partitioning, in order to facilitate dataflow satisfying the temporal needs of the device.

The ASIC floor planning activity shall result in the placement planning of ASIC I/O and major functional blocks (including hard IP).

5.4.9.2 ASIC Place and Route

The purpose of the ASIC place and route activity is to populate the synthesized gates and routing within the confines of the die to produce a final circuit layout.

The ASIC place and route activity shall result in:

a. Generation of the I/O ring
b. Placement and routing of the synthesized gates
c. Placement and routing of memory
d. Final implementation of design for test features
e. Synthesis of clock and reset trees
f. Definition of the power and ground buses
g. Final artwork description (e.g., GDSII file)

5.4.9.3 ASIC Circuitry Analysis

The purpose of the ASIC circuitry analysis activity is to analyze the physical design to ensure that it meets all ASIC circuit power, grounding, timing, and signaling criteria.

The ASIC physical design circuitry analysis activity shall analyze the design and result in:

a. Logic simulations of the design's final net list
b. Logical equivalency assessment of the final design/net list
c. Static timing analysis of the final design/net list
d. Power estimation of the final design/net list
e. Final design area use compared to device capacity, manufacturer's recommended maximum use, and developer's risk threshold metrics (e.g., 80% of manufacturer's recommended maximum)
f. Final design gate count compared to device gate count capacity, manufacturer's recommended gate count, and developer's gate count risk threshold metrics (e.g., 80% of manufacturer's recommended maximum)

In addition, the final design shall be subjected to foundry process rule checks, including Design Rule Check (DRC), Electrical Rule Check (ERC), Layout vs. Schematic (LVS), antenna rule checks, noise rule checks, and power droop rule checks. The design shall also meet all foundry criteria for Simultaneously Switching Outputs (SSO), power consumption, and maximum operating temperature constraints.

5.4.9.4 ASIC CDR and RTM

The ASIC physical design activity shall conclude with the completion of an ASIC Critical Design Review (CDR) and the approved design's Release to Manufacturing.

Each ASIC CDR shall include:

a. Review of final architecture
b. Review of packaging and I/O requirements

c. Review of final power consumption
d. Review for grounding
e. Review of extent that the design will satisfy functional and performance requirements
f. Review of design margins, including final timing margins
g. Review of final design resource utilizations (e.g., area, gate count)
h. Review of final design for test
i. Review of test metrics
j. Final version description
k. Review of foundry checklist compliance

ASIC CDR non-technical content and format requirements are in Appendix A.

The original ASIC CDR presentation material and any revisions, ASIC CDR action items, and ASIC PDR action item responses shall be archived in the product development library.

A memorandum describing the justification for approving the ASIC design's release to manufacturing shall be archived in the product development library.

Section 6.3 contains information regarding the ASIC CDR DID.

5.5 Design Verification

5.5.1 ASIC/FPGA Interface Circuit Analysis

The developer shall perform and document an ASIC/FPGA interface circuit electrical analysis.

The purpose of the ASIC/FPGA interface circuit analysis activity is to provide evidence that the circuitry was designed with adequate grounding, power and signaling characteristics and margin to meet the technical and contractual requirements.

5.5.1.1 ASIC/FPGA Circuit Analysis Report

The ASIC/FPGA circuit analysis activity shall result in an ASIC/FPGA circuit design analysis report (CDAR). At a minimum, the contents of the CDAR shall include the results from the ASIC/FPGA circuit analyses for the subject circuitry (for an FPGA see section 5.4.8.1; for an ASIC see section 5.4.9.3) and any recommendations necessary to correct identified deficiencies and to ensure requirement compliance.

CDAR non-technical content and format requirements are in Appendix A.

The original CDAR and any revisions shall be archived in the product development library.

Information regarding the CDAR DID is in Section 6.3.

5.5.2 Type II ASIC/FPGA Emulation and Demonstration

5.5.2.1 Type II ASIC/FPGA Emulation

In advance of committing to a final Type II ASIC/FPGA design configuration, the developer shall implement the Type II ASIC/FPGA using one or more PLD and subject the implementation to a comprehensive suite of design verification tests. The PLD(s) used shall have performance

characteristics that are equivalent, as closely as possible, to the end item ASICs and/or FPGAs. The design verification test configuration shall include a high fidelity representation of the parent item integrated with the PLD(s) emulating the end item Type II ASIC/FPGA. With the exception of adjustments to accommodate PLD constraints, the Type II ASIC/FPGA circuit definitions used to demonstrate design verification satisfaction shall be the final version of those definitions.

Any software and/or firmware executed by a processor embedded within a Type II ASIC/FPGA shall be a high fidelity representation of the final version of that processor software and/or firmware.

The purpose of the Type II ASIC/FPGA emulation activity is to minimize circuit design risk by ensuring that the ASIC/FPGA system performs in satisfaction of its requirements when operating with its parent item.

5.5.2.2 Parent Item Fidelity

When possible, the PLD(s) used to emulate the ASIC and/or FPGA shall be integrated with the parent item having characteristics equivalent to its final configuration; otherwise, the parent item interface, behavioral and performance characteristics shall be as close as possible to it final configuration.

5.5.2.3 Verification Test Suite

The verification test suite shall be capable of satisfying all of the requirements in the RVTM that can be satisfied by test and/or demonstration. The testing shall be comprehensive, representative of the intended uses, and in accordance with the contract requirements.

5.5.2.4 ASIC/FPGA Emulation and Demonstration Report

The ASIC/FPGA emulation activity shall result in an ASIC/FPGA emulation and demonstration report (AFER) that includes:

a. Overview of ASIC/FPGA emulation plan, architecture and modeling
b. Description of the test assumptions
c. Description of the test configuration
d. List of differences between the actual and the emulation system
e. Description of the test scenarios
f. List of requirements with an indication of which were tested and which were not tested
g. Results of tests
h. Risk of committing the circuitry tested to the final design
i. Test conclusions

AFER non-technical content and format requirements are in Appendix A.

The original AFER and any revisions shall be archived in the product development library.

Information regarding the AFER DID is in Section 6.3.

5.6 End Item ASIC/FPGA Integration and Qualification

5.6.1 End Item ASIC/FPGA and Parent Item Integration

The developer shall integrate the ASIC/FPGA end item (e.g., final) design configuration with the end item design configuration of its parent item and subject them to a comprehensive suite of design verification tests.

Any software and/or firmware executed by a processor embedded within an ASIC/FPGA shall be a high fidelity representation of the final version of that processor software and/or firmware.

5.6.1.1 Integrated ASIC/FPGA and Parent Item Verification Tests

The suite of ASIC/FPGA and parent item integration verification tests shall be capable of satisfying all of the requirements in the RVTM that can be satisfied by test and/or demonstration. The testing shall be comprehensive, representative of the intended uses, and in accordance with the contract requirements.

5.6.1.2 ASIC/FPGA and Parent Item Integration Report

The end item ASIC/FPGA and parent item integration activity shall result in a parent item integration report (PIR) that reports the following information about the end item ASIC/FPGA and parent item integration and testing:

a. Description(s) of the test configuration(s)
b. Listing of any test assumptions applied to the integration and testing
c. Listing of the test scenarios and test cases applied to the testing
d. Listing of any requirements of functions that were not tested
e. Test conclusions
f. Description(s) of any risks of committing the ASIC/FPGA to qualification testing

PIR non-technical content and format requirements are in Appendix A.

The original PIR and any revisions shall be archived in the product development library.

Information regarding the PIR DID is in Section 6.3

5.6.2 Parent Item Qualification

The developer shall subject the personalized ASIC/FPGA to qualification testing.

5.6.2.1 Qualification Tests

The personalized ASIC/FPGA qualification tests, in conjunction with any supporting analyses, shall verify all of the ASIC/FPGA requirements in the RVTM, applicable AFSS, and the contract.

5.6.2.2 Qualification Test Report

The qualification test used to qualify the personalized ASIC/FPGA in its end item configuration shall be documented in a qualification test report (QTR).

A QTR shall include:

a. Description of items(s) under test
b. Identification of configuration items used in the test (e.g., devices(s), FPGA configuration file, software)
c. Description of the tests and test environment(s)
d. Description of performance deficiencies and a description of their close-out rationale
e. Description of final test results
f. Copy of the as-run test procedure

QTR non-technical content and format requirements are in Appendix A.

The original QTR and any revisions shall be archived in the product development library.

Information regarding the QTR DID is in Section 6.3

5.7 FPGA Post-Qualification Changes and Verification

All post-qualification changes shall be subject to the planning, development, verification, integration, qualification, reporting and documentation requirements specified herein.

A new or changed FPGA configuration file shall have been loaded into its parent item and subjected to a complete, comprehensive and successful parent-item qualification/re-qualification test prior to loading the new or changed FPGA configuration file into system (e.g., flight) hardware. [Note: While the qualification/re-qualification must include ambient and thermal testing, other environmental testing may be omitted if so approved by the acquirer.]

5.8 Peer Reviews

The developer shall plan, establish guidelines for, perform, document and analyze the results of peer reviews of the following ASIC/FPGA development work products:

a. AFDP
b. Requirements
c. Design decisions
d. ASIC/FPGA circuit design source code
e. ASIC/FPGA verification test cases
f. ASIC/FPGA emulation and verification results
g. ASIC/FPGA analyses
h. Qualification test results
i. Reports (i.e., CDAR, AFER, PIR, QTR)

Minutes from the peer reviews shall be documented and archived in the product development library.

5.9 Subcontractor Management

When subcontractors are used, the developer shall include in subcontracts all contractual requirements necessary to ensure that ASIC/FPGA circuit modules and associated development products are developed in accordance with prime contract requirements.

6. Notes

This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.

6.1 Intended Use

This standard is intended to be applied to contracts wherein ASIC/FPGA digital circuitry is developed and/or maintained.

6.2 Acquisition Requirements

Digital application-specific integrated circuit and field-programmable gate array circuit development for space systems; Aerospace Report TOR-2010(8591)-10.

6.3 Technical Data Items and Associated DIDs

In order to have technical data items delivered under the contract, they must be included on the Contract Data Requirements List (CDRL) and associated with a Data Item Description (DID). The following table correlates key technical data items identified in this standard to recommend DIDs that could be referenced in a CDRL item intended to order the technical data item delivery to the acquirer.

Technical Data Item	Recommended DID #	Paragraph
ASIC/FPGA development plan (AFDP)	DI-MISC-80711A	5.1.1.1
ASIC/FPGA system specification (AFSS)	DI-CMAN-80776 *	5.2.1; Preliminary 5.3.5; Final
Requirement verification and traceability matrix (RVTM)	DI-CMAN-80776 *	5.2.2; Draft 5.3.6; Preliminary 5.4.6; Final
Consolidated requirements review (CRR)	DI-ILSS-81335 *	5.2.3
ASIC/FPGA circuit design specification	DI-CMAN-80776 *	5.3.3; Preliminary
Final requirements review (FRR)	DI-ILSS-81335 *	5.3.8
ASIC/FPGA Preliminary Design Review (PDR)	DI-ILSS-81335 *	5.4.5
FPGA Critical Design Review (CDR)	DI-ILSS-81335 *	5.4.8.3
ASIC Critical Design Review (CDR)	DI-ILSS-81335 *	5.4.9.4
Circuit design analysis report (CDAR)	DI-MISC-80711A	5.5.1.1
ASIC/FPGA emulation report (AFER)	DI-MISC-80711A	5.5.2.4
ASIC/FPGA system and Parent item integration report (PIR)	DI-MISC-80711A	5.6.1.2
Qualification test report (QTR)	DI-MISC-80711A	5.6.2.2

*may require tailoring

6.4 Tailoring Guidance

This standard and its DIDs are applied at the discretion of the acquirer. In each application, the standard and DIDs should be tailored to the specific requirements of a particular program, program phase, or contractual structure. Care should be taken to eliminate tasks that add unnecessary costs and data that do not add value to the process or the product. Tailoring for the standard takes the form of deletion of activities, alteration of activities to more explicitly reflect the application to a particular effort, or addition of activities to satisfy program requirements. This tailoring is specified in the Statement of Work (SOW) or Compliance Document section of the contract. Tailoring the DIDs consists of deleting requirements for unneeded information and making other changes, such as combining two documents under one cover, that do not increase the required workload. DID tailoring for deliverables is specified in the Contract Data Requirements List (CDRL).

Appendix A. Non-technical Content and Format Requirements for Key Development Documentation Artifacts

A.1 Scope

Appendix A provides the necessary, non-technical content and format requirements for the following ASIC/FPGA development products:

a. ASIC/FPGA development plan (AFDP)
b. ASIC/FPGA system specification (AFSS)
c. Requirement verification and traceability matrix (RVTM)
d. Consolidated requirements review (CRR)
e. ASIC/FPGA circuit design specification
f. Final requirements review (FRR)
g. ASIC/FPGA Preliminary Design Review (PDR)
h. FPGA Critical Design Review (CDR)
i. ASIC Critical Design Review (CDR)
j. Circuit design analysis report (CDAR)
k. ASIC/FPGA emulation report (AFER)
l. ASIC/FPGA system and Parent item integration report (PIR)
m. Qualification test report (QTR)

This Appendix is a mandatory part of the standard. The information contained herein is intended for compliance.

A.2 Key ASIC/FPGA Development Documentation Artifact Non-technical Content and Format Requirements

A.2.1 ASIC/FPGA Development Plan (AFDP) Content and Format

In addition to contractually required content, the AFDP shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the AFDP shall be clearly written, technically accurate and presented using the developer's format.

A.2.2 AFSS Content and Format

In addition to contractually required content, the AFSS shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the AFSS shall be clearly written, technically accurate and presented using the developer's format.

A.2.3 RVTM Content and Format

In addition to contractually required content, the RVTM shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the RVTM shall be clearly written, technically accurate and presented using the developer's format.

A.2.4 Consolidated Requirements Review (CRR) Content and Format

In addition to contractually required content, a CRR shall include:

a. Program or project identification
b. Document title, number, revision, and release date

Unless otherwise specified by the contract, the CRR shall be clearly written, technically accurate and presented using the developer's format.

A.2.5 ASIC/FPGA Circuit Design Specification Content and Format

In addition to contractually required content, each ASIC/FPGA circuit design specification shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, each ASIC/FPGA circuit design specification shall be clearly written, technically accurate presented using the developer's format.

A.2.6 Final Requirements Review (FRR) Content and Format

In addition to contractually required content, each FRR shall include:

a. Program or project identification
b. Document title, number, revision, and release date

Unless otherwise specified by the contract, each FRR shall be clearly written, technically accurate and presented using the developer's format.

A.2.7 ASIC/FPGA PDR Content and Format

In addition to contractually required content, each ASIC and FPGA PDR shall include:

a. Program or project identification
b. Document title, number, revision, and release date

Unless otherwise specified by the contract, each ASIC and FPGA PDR shall be clearly written, technically accurate and presented using the developer's format.

A.2.8 FPGA CDR Content and Format

In addition to contractually required content, each FPGA CDR shall include:

a. Program or project identification
b. Document title, number, revision, and release date

Unless otherwise specified by the contract, each FPGA CDR shall be clearly written, technically accurate and presented using the developer's format.

A.2.9 ASIC CDR Content and Format

In addition to contractually required content, each ASIC CDR shall include:

a. Program or project identification
b. Document title, number, revision, and release date

Unless otherwise specified by the contract, each ASIC CDR shall be clearly written, technically accurate and presented using the developer's format.

A.2.10 Circuit Design Analysis Report (CDAR) Content and Format

In addition to required content, a CDAR shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the CDAR shall be presented using the developer's format.

A.2.11 ASIC/FPGA Emulation and Demonstration Report (AFER) Content and Format

In addition to contractually required content, an AFER shall include:

a. Program or project identification
b. Document title, number, revision, and release date

c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the AFER shall be presented using the developer's format.

A.2.12 Parent Item Integration Report (PIR) Content and Format

In addition to contractually required content and formatting, a PIR shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Scope description
f. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the PIR shall be presented using the developer's format.

A.2.13 Qualification Test Report (QTR) Content and Format

In addition to contractually required content and formatting, a QTR shall include:

a. Program or project identification
b. Document title, number, revision, and release date
c. Table of contents
d. List of applicable documents
e. Definitions of acronyms and technical terms

Unless otherwise specified by the contract, the QTR shall be presented using the developer's format.

Appendix B. Overview of this Standard's Major Sections of Detailed Requirements Correlated to Development Artifacts and ASIC/FPGA Type

B.1 Scope

Appendix B provides an overview, in the form of a table, of the major sections of the detailed requirements of the standard (on the left) correlated to the development artifacts each section requires (on the right) by ASIC/FPGA type.

B.2 Table of Major Sections of Detailed Requirements Correlated to Key Development Artifacts and ASIC/FPGA Type

Detailed Requirements Sections	Key ASIC/FPGA development artifacts required to be produced	
	Type I ASIC/FPGA	Type II ASIC/FPGA
5.1 Project planning preparation and coordination	• AFDP	• AFDP
5.2 Parent item and relevant requirements analysis and flow-down	• RVTM, draft • CRR	• AFSS, preliminary • RVTM, draft • CRR
5.3 ASIC/FPGA requirements and architecture definition	• Trade studies and design decisions • ASIC/FPGA device selection • ASIC/FPGA architecture • ASIC/FPGA circuit design specification(s) • RVTM, preliminary • FRR	• Trade studies and design decisions • ASIC/FPGA device selection • ASIC/FPGA architecture • ASIC/FPGA circuit design specification(s) • Explicit SW requirements • AFSS, final • RVTM, preliminary • FRR

5.4 ASIC/FPGA circuit development and verification	• ASIC/FPGA circuit source code
	• Circuit verification metrics
	• Verification source code
	• PDR
	• RVTM, final
	• FPGA
	  • Circuit analysis
	  • Configuration file
	  • CDR
	• ASIC
	  • Physical design
	  • Circuit analysis
	  • CDR & RTM
		• ASIC/FPGA circuit source code
		• Circuit verification metrics
		• Verification source code
		• PDR
		• RVTM, final
		• FPGA
		  • Circuit analysis
		  • Configuration file
		  • CDR
		• ASIC
		  • Physical design
		  • Circuit analysis
		  • CDR & RTM

5.5 Design verification	• Interface circuit analysis & CDAR	• Interface circuit analysis & CDAR • Type II (with SW) emulation, demonstration and AFER
5.6 End item ASIC/FPGA integration and qualification	• ASIC/FPGA Parent item integration and PIR	• ASIC/FPGA Parent item integration and PIR

	• Parent item qualification & QTR	• Parent item qualification & QTR
5.7 FPGA Post-Qualification Changes and Verification	• Change dependent updates to various artifacts shown above	• Change dependent updates to various artifacts shown above
5.8 Peer Reviews	• Minutes	• Minutes
5.9 Subcontractor Management	• Flow down and management of contractual requirements	• Flow down and management of contractual requirements

Table B.1. Major sections of detailed requirements and their required development artifacts.